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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/678,527	10/03/2003	Roland A. Wood	H0001861 (1100.1214101)	1355

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EXAMINER	
ZETTL, MARY E	
ART UNIT	**PAPER NUMBER**
2878	

DATE MAILED: 09/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/678,527	WOOD ET AL.	
	Examiner	Art Unit	
	Mary Zettl	2878	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/04 and 8/05* .
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. The term "small area" in claims 8 and 20 is a relative term which renders the claim indefinite. The term "small area" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-19 and 23-29 are rejected under 35 U.S.C. 102(b) as being anticipated by Gates (US 5,554,849).

5. Regarding Claims 1-10, Gates discloses a micro-bolometric infrared sensor (Abstract) comprising a substrate (Figure 4, item 26; Column 2, line 53) with a pit (trench) proximate to a pixel (Figure 4, item 24; Column 6, line 14); a pixel situated on a single level on the substrate (Column 2, line 52); and an electronics circuit (Figure 3, items 30 and 32; Column 7, lines 62-67). Gates further discloses a fill factor greater than fifty percent (Column 8, line 49). The pixel is further disclosed as being an infrared light detector (Abstract). Gates further discloses at least one via in the one level (wafer

or device that contains the bolometric array) supporting the pixel (Column 8, lines 35-38). Additionally Gates discloses the electronics circuitry (switch pixel address mechanism) disclosed in Claim 1, is typically a FET or bipolar transistor circuit (Column 1, line 37), or CMOS (Column 8, lines 44-45).

6. Regarding Claims 11-15, Gates discloses a thermal sensor comprising: a substrate (Figure 4, item 26; Column 2, line 53); and an array of pixels (Column 2, lines 51-53), situated on the substrate, over a pit(Figure 4, item 24; Column 6, line 14); and wherein: each pixel is located on a single level; an electronic circuit is associated with each pixel; and each electronic circuit is CMOS FET circuitry (Column 1, line 37 and Column 8, lines 44-45) and is located on the single level with the pixel. In addition Gates discloses that each pixel is an infrared light detector (Abstract) and a microbolometer (Abstract).

7. Regarding Claims 16-19, Gates discloses a sensing means comprising a means for sensing infrared light (Abstract), a means for electronically processing signals related to infrared light sensed by the means for sensing infrared light (Figure 3, items 30 and 32; Column 7, lines 62-67), and a means for supporting on one level the means for sensing infrared light and the means for electronically processing signals, where the means for supporting on one level supports the means for sensing infrared light over a thermal isolating opening (Figure 2, item 24; Column 4, line 65-66). Gates further discloses that the means for sensing infrared light is an array of pixels (Abstract) and that the means for electronically processing signals has an area that is a fraction of the

area of the means for sensing infrared light (indicated by a fill factor greater than fifty percent; Column 8, line 49).

8. Regarding Claim 23, Gates discloses a sensor comprising: a substrate (Figure 4, item 26; Column 2, line 53); a pixel situated in a first plane relative to a surface of the substrate (Column 2, line 52); and an electronics circuit situated in the first plane (Figure 3, items 30 and 32; Column 7, lines 62-67).

9. Regarding Claim 24, Gates discloses a thermal sensor comprising: a substrate (Figure 4, item 26; Column 2, line 53); and an array of pixels situated on the substrate (Column 2, line 52); and wherein: each pixel is located on a first surface (Column 5, lines 58-60); an electronic circuit is associated with each pixel; and each electronic circuit is located on the first surface proximate to the pixel (Column 7, lines 62-67 and Column 8, lines 35-38).

10. Regarding Claim 25, Gates discloses a thermal sensor comprising: a substrate (Figure 4, item 26; Column 2, line 53); and an array of pixels situated on the substrate (Column 2, line 52); and wherein: an electronic circuit is associated with each pixel (Column 7, lines 62-67); and each electronic circuit is situated horizontally proximate to the pixel (Column 7, lines 62-67 and Column 8, lines 35-38).

11. Regarding Claim 26, Gates discloses a thermal sensor comprising: a substrate (Figure 4, item 26; Column 2, line 53); and an array of pixels situated on the substrate (Column 2, line 52); and electronics situated on the substrate horizontally proximate to the array of pixels (Figure 3, items 30 and 32; Column 7, lines 62-67).

12. Regarding Claim 27 , Gates discloses a sensing means comprising: means for sensing infrared light (Abstract); means for electronically processing signals related to infrared light sensed by the means for sensing infrared light (Figure 3, items 30 and 32; Column 7, lines 62-67); and a means for supporting on one surface the means for sensing infrared light and the means for electronically processing signals (Column 8, lines 35-38).

13. Regarding Claim 28, Gates discloses a sensing means comprising: means for sensing infrared light (Abstract); means for electronically processing signals related to infrared light sensed by the means for sensing infrared light (Figure 3, items 30 and 32; Column 7, lines 62-67); and a means for sensing infrared light and the means for electronically processing signals horizontally proximate each other (Column 8, lines 35-38).

14. Regarding Claim 29, Gates discloses a sensing means comprising: means for sensing infrared light (Abstract); means for electronically processing signals related to infrared light sensed by the means for sensing infrared light (Figure 3, items 30 and 32; Column 7, lines 62-67); and a means for supporting in a plane the means for sensing infrared light and the means for electronically processing signals (Column 8, lines 35-38).

15. Claim 1 and Claims 11-13 are further rejected under 35 U.S.C. 102(b) as being anticipated by Wood et. al (US 5,449,910).

16. Regarding Claim 1, Wood discloses a sensor comprising substrate (base of silicon material; Figure 2, item 64; Column 3, line 60); a pixel situated on a single level

on the substrate (Figure 2, item 10; Column 3, line 52); and an electronics circuit situated on the single level (Figure 2, item 57; Column 3, lines 66-70 – Column 4, lines 1-4).

17. Regarding Claims 11-13, Wood discloses a thermal sensor (Abstract) comprising a substrate (base of silicon material; Figure 2, item 64; Column 3, line 60); an array of pixels functioning as infrared light detectors (Abstract) which are situated on a single level of the substrate (Figure 2, item 10; Column 3, line 52); with an electronic circuit associated with each pixel and located on the single level (Figure 2, item 57; Column 3, lines 66-70 – Column 4, lines 1-4). Wood further discloses that each pixel is suspended over a pit in the substrate (Figure 2, item 24; Column 4, line 65).

Claim Rejections - 35 USC § 103

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

19. Claim 20, 21, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gates (US 5,554,849) and in view of Cole et al. (US 6,313,463).

Gates teaches all of the limitations set forth in Claim 19. Gates further teaches the means for supporting the sensing means on one level is a planar level substrate (Figure 4; item 26; Column 2, line 52); a thermal isolating opening in a substrate under

each pixel of an array of pixels (Figure 4, item 24; Column 6, line 14); and an array of pixels being a microbolometer (Abstract), and CMOS FET transistor circuitry (Column 1, lines 36-38 and Column 8, lines 44-45). Gates does not expressly disclose a microbolometer pixel comprising VOx. Cole teaches a microbolometer in which a pixel contains the material VOx (Abstract). VOx is a common electrical insulating material used in pixels because of its thermal resistance to the flow of heat along the plane. Cole further teaches that VOx detector material has optical, electrical, and thermal properties compatible with high performance detectors that can also be readily modified to suit individual requirements of an array design (Column 1, lines 47-50). At the time the invention was made it would have been obvious to a person of ordinary skill in the art to modify the pixels disclosed by Wood and Gates by fabricating them out of VOx as suggested by Cole since VOx is a common pixel fabrication material having a desirable thermal resistance and desirable optical, electrical, and thermal properties.

Conclusion

20. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Iida et al. (US 6,806,470) – this reference teaches an infrared sensor (Figures 1-4, Column 6, line 44) comprising a pixel (Figure 2, item 20; Abstract) and a MOS transistor associated with each pixel (Figure 2, item 61; Column 7, lines 24-25) situated on the single level of a substrate (Figure 2, item 11; Column 6, line 53) which has a pit proximate to the pixel (Figure 2, item 160). This reference further teaches that the thermoelectric conversion means could be a bolometer (Column

16, lines 64-67). Iida further teaches the means for electronically processing signals having an area that is a fraction of the area of the means for sensing infrared light (Figure 2). Iida further teaches the electronic circuit is located on a first surface, situated horizontally proximate to the pixel

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mary Zettl whose telephone number is (571) 272-6007. The examiner can normally be reached on M-F 8am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Porta can be reached on (571) 272-2444. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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